FPGA based flexible UWB pulse transmitter using EM subtraction

M. Strackx, B. Faes, E. D'Agostino, P. Leroux and P. Reynaert

An all-digital field programmable gate array based electromagnetic subtraction technique for direct UWB pulse generation is presented. Using this technique, it is possible to generate Gaussian pulses, monocycles or doublets with high flexibility using a single printed circuit board layout. User-controlled parameters include amplitude, pulse-width, pulse-type, repetition rate or even modulation. Measurements indicate a Gaussian pulse with 1.24 V peak amplitude and a 10% pulse-width of 670 ps can be transmitted at a repetition frequency of 100 MHz. The corresponding − 10 dB bandwidth is 2.8 GHz.

Introduction: Over the past decade, UWB radio has been commonly proposed for short-range high data rate communications [1] or for radar applications in the industrial [2] and medical fields. However, widespread implementation is still ongoing. This Letter contributes to providing an easy implementable development platform for UWB signal generation with higher flexibility compared with other transmitters. The key innovation of the Letter is the usage of a field programmable gate array (FPGA) together with an electromagnetic (EM) subtraction technique to form different Gaussian pulse shapes in a direct way. Two general transmitter implementations exist to date. CMOS integrated circuits can be considered for full-custom designs, while on the other hand, transmitters can be composed using commercial off-the-shelf components. The latter are implemented with step recovery diodes (SRDs) [2] or mesfets to generate steep edges and provide flexibility to some extent. An all-digital FPGA based implementation combines the high flexibility of CMOS designs together with rapid and easy implementation.

Architecture: The architecture of the pulse generator is presented in Fig. 1. An external clock signal controls the pulse repetition frequency of the transmitted UWB pulses. For optional increased flexibility, it is also possible to use a frequency synthesiser of the FPGA to change this parameter. The clock signal is used internally to drive a digital clock manager (DCM) which includes a phase locked loop to lower the jitter at the output and to generate several out-of-phase components. The phase shifts of each DCM output can be controlled on-the-fly. In this way, the DCM can be considered as a digital-to-time converter (DTC) which benefits from CMOS scaling. When using a more recent technology node, timing resolution will increase. Also, depending on the application, it is possible to choose a different FPGA with a higher or lower timing resolution. Each pair of DCM outputs is combined in a glitch generator which has both reconfigurable rising and falling edges. Each glitch can now be shifted over time as well as have an adjustable pulse-width.

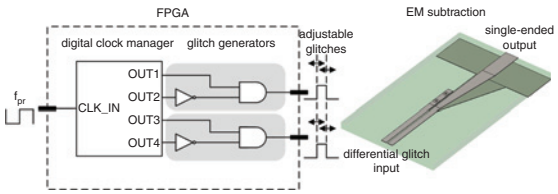

Fig. 1 *Block diagram of FPGA based UWB pulse transmitter with EM subtraction on PCB level using CPS to MS transition*

EM subtraction: Both glitches are transmitted by a differential coplanar stripline (CPS) which supresses the common mode component and passes through the differential one. Mathematically, this is the equivalent of a subtraction. One of the striplines is connected to the bottom side of the printed circuit board (PCB) and forms the new ground plane of the microstrip (MS) transmission line. Both the ground plane and other stripline are linearly tapered to minimise insertion and reflection losses. A general mathematical understanding of this type of transition is given in [3]. Compared to [3], the transition is altered for the UWB application using the following adjustments: linear tapering profiles, less vias and tapering of the top stripline. Full-wave EM simulations indicate a return loss better than 10 dB in the 1.5–10 GHz band with an insertion loss of less than 2 dB on an FR4 substrate. Using the proposed EM subtraction technique, the pulse generator is capable of generating Gaussian pulses, monocycles and doublets with the same architecture. The different pulses are generated based on user adjustable time delays. Fig. 2 shows the operating principle of the proposed EM subtraction technique to form different kinds of pulse shapes. The amplitude of the generated pulses can also be controlled by adjusting the slew-rate setting of the FPGA. For doublet generation, an additional pair of DCM outputs is added in combination with a glitch generator. Two glitch generator outputs then need to be combined using an OR gate for $IN-$. For better FCC compliant pulse generation, a voltage controlled oscillator was added in a second test structure with a mixer for frequency translation. The oscillation frequency can also be controlled from the FPGA, providing additional flexibility. The maximum centre frequency for up-conversion is 5.5 GHz in this design.

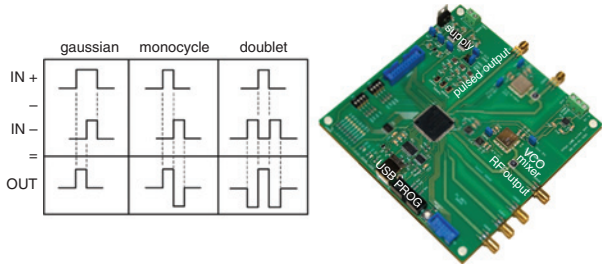

Fig. 2 *EM subtraction technique for Gaussian pulse generation and PCB of FPGA based UWB transmitter*

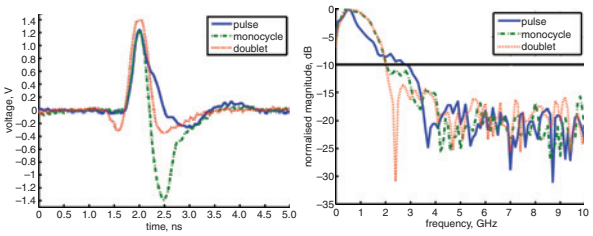

Fig. 3 *Measured Gaussian pulse, monocycle and doublet in time and frequency domains*

Measurement results: The FPGA output is directly connected via the CPS-MS transition to a high-frequency oscilloscope. The measured UWB pulses are shown in Fig. 3, both in the time and frequency domains. These are generated using the smallest time offset and highest slew-rate setting on a Xilinx Spartan 6 FPGA to show the performance. Wider pulses with narrower frequency content can easily be generated with larger time offsets. The measured Gaussian pulse has a 10% pulse-width of 670 ps with a peak amplitude of 1.24 V, achieving a 10 dB bandwidth of 2.8 GHz. The Gaussian monocycle has a 10% pulse-width of 1.48 ns with a peak-to-peak amplitude of 2.64 V, achieving a 10 dB bandwidth of 2.0 GHz. The Gaussian doublet has a 10% pulse-width of 1.67 ns with a peak-to-peak amplitude of 1.74 V, achieving also a 10 dB bandwidth of 2.0 GHz. These signals indicate the high flexibility of the transmitter. However, the generated pulses still have some low-frequency components which are difficult to transmit with small UWB antennas. For this reason, an additional up-conversion can be performed to 5.5 GHz as an example. The example up-converted pulse is shown in Fig. 4, both in the time and frequency domains. The pulse has a 10% width of 2.02 ns with a peak-to-peak amplitude of 482 mV, achieving a 10 dB bandwidth of 2.3 GHz. The signal energy present in the 1–1.6 GHz band can be further reduced using a proper UWB antenna or filter. Table 1 lists all of the measured parameters and compares the performance with the 65 nm CMOS [1], SRD on PCB [2], 0.13 µm CMOS [4] and 0.18 µm CMOS [5, 6] designs. Compared with the CMOS designs, similar performance is achieved. Compared with the PCB designs with discrete components, higher flexibility is demonstrated.

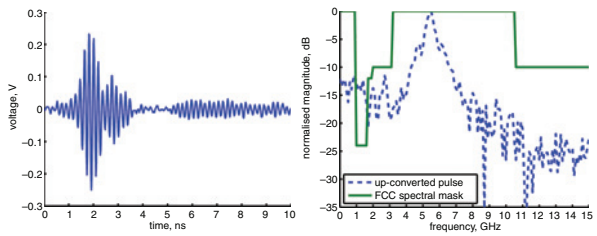

Fig. 4 *Measured up-converted pulse in time and frequency domains for transmission with UWB antennas*

Table 1: Performance comparison to prior work

Ref.	$T_{10\%}$	V_{ptp}	$f_{-10\,dB}$ (GHz)	f_c (GHz)	Type
[1]	2.5 ns	91 mV	1.4	5	up-converted
[2]	450 ps	5.8 V	3.7	—	monocycle
[4]	1.0 ns	240 mV	2	4	higher order
[5]	500 ps	673 mV	4.5	8.2	up-converted
[6]	1.75 ns	1.25 V	1.4	4.1	higher order
This work	670 ps	1.24 V	2.8	0.5	Gaussian pulse
This work	1.48 ns	2.64 V	2.0	0.5	monocycle
This work	1.67 ns	1.74 V	2.0	0.7	doublet
This work	2.02 ns	482 mV	2.3	5.5	up-converted

Conclusion: This Letter presents an FPGA based flexible UWB pulse transmitter. Using the proposed EM substraction technique, Gaussian pulses, monocycles and doublets can be generated by a single transmission line structure on the PCB. Owing to the high flexibility, this technique offers a rapid prototyping alternative compared with CMOS designs. As a proof-of-concept, an up-conversion is also performed such that the generated pulses can be transmitted with antennas and comply with the spectral emission limits.

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One or more of the Figures in this Letter are available in colour online.

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